

paths. Any stray signals that enter the buddy traces will therefore be sent to ground and not cause distortion. This greatly enhances the integrity of the signals along the bus lines.

Figure 5 also shows a close up view of some signal paths. In this figure it can be seen that the RSL traces are 110 um and the buddy traces are 35um. This embodiment also shows that the spacing between the buddy traces and the RSL lines to be 35 um. It is also shown that the RSL lines change their width from 110 um to 35 um. It is this changing of signal path widths that embodies the present invention. As also seen in Figure 4, for a length of 3.2 mm, the signal path just before entering the chip is reduced in width to 35 um.

Figure 6 shows signal path CMOS lines that are 35 um in width with a spacing of 78.1 um between CMOS lines.

Figure 7 shows other CMOS signal paths that have adjacent buddy traces. In this area of the bus, the CMOS lines are 35 um in width with the buddy traces also being 35 um in width. The spacing is shown at 62.5 um in this embodiment.

It is noted that all prior art methods of bus connections do not approach the method taught by the present invention. It is common knowledge that problems with high speed busses existed, however no exact means to compensate for this has been determined until the present invention.

Finally, although the present invention has been described in accordance with the shown embodiments, variations to the embodiments would be apparent to those skilled in the art and those variations would be within the scope and spirit of the present invention. Accordingly, it is intended that the specification and embodiments shown be considered as
5 exemplary only, with a true scope of the invention being indicated by the claims that follow and equivalents.